(19) Japan Patent Office (JP)
(12) Publication of Unexamined Patent Application (A)
(11) Japanese Patent Laid-Open Number: Tokkai Hei 5-218464
(43) Laid-Open Date: Heisei 5-.-27 (August 27, 1993)
(51) Int.Cl.[5] Identification Code F1 Theme Code(reference)
H01L 31/04 9171-4M
21/20 7376-4M H01L 31/04 A
7376-4M X
Request for Examination: Not Requested
Number of Claims: 20
(24 pages in total)
(21) Number Assigned to the Application: Tokugan Hei. 4-16506
(22) Date of Filing Application: Heisei 4-1-31 (January 31, 1993)
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(54) Title of the Invention: METHODS OF MANUFACTURING SEMICONDUCTOR BASE BODY AND SOLAR CELL, AND SEMICONDUCTOR BASE BODY AND SOLAR CELL OBTAINED BY THESE METHODS

(57) [Abstract]
[Object]
To provide a semiconductor substrate having a high-quality epitaxial Si layer formed on a metal substrate, and a method of manufacturing a thin-film crystalline solar cell using the same.
[Construction]
A porous Si layer 102 is formed through anodization on a Si wafer 101. A surface of a non-single crystalline Si layer 104 deposited on a metal substrate 103 is brought into contact with a surface of the porous Si layer 102. Then, heat treatment is carried out for solid-phase growth, and thus the porous Si layer grows as seed crystal to turn the non-single crystalline Si layer into a single crystalline silicon layer 106. At the same time, a silicide layer is formed at an interface between the metal substrate 103 and the single crystalline silicon layer. The porous Si is removed through selective etching to separate the Si wafer from the single crystalline silicon layer 106. As a result, a semiconductor substrate with a two-layer structure of metal and single crystalline Si is obtained. Additionally, an epitaxial layer Si 107 is grown epitaxial growth on the single crystalline Si 106, and then a solar cell is formed.

[Scope of Claims]
[Claim 1] A method of manufacturing a semiconductor substrate with a metal/semiconductor two-layer structure, characterized by comprising:

i) a step of depositing a non-single crystalline silicon layer on a metal substrate;

ii) a step of forming a porous surface of a single crystalline silicon substrate;

iii) a step of bringing a surface of the non-single crystalline silicon layer on the metal substrate into contact with a surface of a porous layer on the single crystalline silicon substrate;

iv) a step of turning the non-single crystalline silicon layer opposing the porous layer into single crystal through solid-phase epitaxial growth by means of heat treatment, and at the same time, of forming a silicide layer at an interface between the metal substrate and the non-single crystalline silicon; and

v) a step of removing the porous layer through selective etching to separate the single crystalline silicon substrate from a single-crystallized silicon layer on the metal substrate.

[Claim 2] The method of manufacturing a semiconductor substrate according to claim 1, wherein the non-single crystalline silicon layer is an amorphous silicon layer.

[Claim 3] The method of manufacturing a semiconductor substrate according to claim 1, wherein the porous layer is formed through anodization.

[Claim 4] The method of manufacturing a semiconductor substrate according to claim 1, wherein the selective etching is carried out using a mixture of hydrofluoric acid, alcohol, and hydrogen peroxide solution.

[Claim 5] The method of manufacturing a semiconductor substrate according to claim 1, wherein an impurity is introduced into the non-single crystalline silicon layer any one of during and after the deposition of the non-single crystalline silicon layer.

[Claim 6] A method of manufacturing a solar cell using a solid-phase epitaxial film, characterized by comprising:

i) a step of depositing a non-single crystalline silicon layer on a metal substrate;

ii) a step of forming a porous surface of a single crystalline silicon substrate;

iii) a step of bringing a surface of the non-single crystalline silicon layer on the metal substrate into contact with a surface of a porous layer on the single crystalline silicon substrate;

iv) a step of turning the non-single crystalline silicon layer opposing the porous layer into single crystal through solid-phase epitaxial growth by means of heat treatment, and at the same time forming a silicide layer at an interface between the metal substrate and the non-single crystalline silicon;

v) a step of removing the porous layer through selective etching to separate the single crystalline silicon substrate from a single-crystallized silicon layer on the metal substrate;

vi) a step of forming a silicon epitaxial layer on the single-crystallized silicon layer through thin-film epitaxial growth; and

vii) a step of forming a semiconductor junction on a surface of the epitaxial layer.

[Claim 7] The method of manufacturing a solar cell according to claim 6, wherein the non-single crystalline silicon layer is an amorphous silicon layer.

[Claim 8] The method of manufacturing a solar cell according to claim 6, wherein the porous layer is formed through anodization.

[Claim 9] The method of manufacturing a solar cell according to claim 6, wherein the selective etching is carried out using a mixture of hydrofluoric acid, alcohol, and hydrogen peroxide solution.

[Claim 10] The method of manufacturing a solar cell according to claim 6, wherein an impurity is introduced into the non-single crystalline silicon layer any one of during or after the deposition of the non-single crystalline silicon layer.

[Claim 11] A semiconductor substrate characterized by being manufactured by executing:

i) a step of depositing a non-single crystalline silicon layer on a metal substrate;

ii) a step of forming a porous surface of a single crystalline silicon substrate;

iii) a step of bringing a surface of the non-single crystalline silicon layer on the metal substrate into contact with a surface of a porous layer on the single crystalline silicon substrate;

iv) a step of turning the non-single crystalline silicon layer opposing the porous layer into single crystal through solid-phase epitaxial growth by means of heat treatment, and forming a silicide layer at an interface between the metal substrate and the non-single crystalline silicon; and

v) a step of removing the porous layer through selective etching to separate the single crystalline silicon substrate from a single-crystallized silicon layer on the metal substrate.

[Claim 12] The semiconductor substrate according to claim 11, wherein the non-single crystalline silicon layer is an amorphous silicon layer.

[Claim 13] The semiconductor substrate according to claim 11, wherein the porous layer is formed through anodization.

[Claim 14] The semiconductor substrate according to claim 11, wherein the selective etching is carried out using a mixture of hydrofluoric acid, alcohol, and hydrogen peroxide solution.

[Claim 15] The semiconductor substrate according to claim 11, wherein an impurity is introduced into the non-single crystalline silicon layer any one of during or after the deposition of the non-single crystalline silicon layer.

[Claim 16] A solar cell characterized by being manufactured by executing:

i) a step of depositing a non-single crystalline silicon layer on a metal substrate;

ii) a step of forming a porous surface of a single crystalline silicon substrate;

iii) a step of bringing a surface of the non-single crystalline silicon layer on the metal substrate into contact with a surface of a porous layer on the single crystalline silicon substrate;

iv) a step of turning the non-single crystalline silicon layer opposing the porous layer into single crystal through

solid-phase epitaxial growth by means of heat treatment, and forming a silicide layer at an interface between the metal substrate and the non-single crystalline silicon;

v) a step of removing the porous layer through selective etching to separate the single crystalline silicon substrate from a single-crystallized silicon layer on the metal substrate;

vi) a step of forming a silicon epitaxial layer on the single-crystallized silicon layer through thin-film epitaxial growth; and

vii) a step of forming a semiconductor junction on a surface of the epitaxial layer.

[Claim 17] The solar cell according to claim 16, wherein the non-single crystalline silicon layer is an amorphous silicon layer.

[Claim 18] The solar cell according to claim 16, wherein the porous layer is formed through anodization.

[Claim 19] The solar cell according to claim 16, wherein the selective etching is carried out using a mixture of hydrofluoric acid, alcohol, and hydrogen peroxide solution.

[Claim 20] The solar cell according to claim 16, wherein an impurity is introduced into the non-single crystalline silicon layer any one of during and after the deposition of the non-single crystalline silicon layer.

[Detailed Description of the Invention]
[0001]
[Field of the Industrial Application] The present invention relates to methods of manufacturing a semiconductor substrate and a solar cell. In particular, the present invention relates to methods of manufacturing a substrate having a semiconductor deposited on metal and to methods of manufacturing a solar cell.
[0002]
[Prior Art] In times of cost-consciousness, a photoelectric conversion element, especially a solar cell, is preferably formed on an inexpensive substrate, such as a metal substrate, especially, one of SUS. How to form a high-quality semiconductor layer on metal is important for this purpose.
[0003] As a semiconductor constituting a solar cell, silicon is ordinarily used, and single-crystalline silicon, polysilicon, and amorphous silicon are forms thereof. In order to get larger area and to save costs, amorphous silicon is considered to be advantageous. However, it is preferable to use single-crystalline silicon in view of efficiency in conversion of light energy into electromotive force, and in view of stability. In recent years, the use of polysilicon has been under study for the purpose of lowering costs down to the level as in the case of using amorphous silicon, and for the purpose of attaining high efficiency in energy conversion up to the level as in the case of using single crystalline silicon. In conventional technology, a massive crystal of single crystalline or polysilicon is sliced into slices for use. A slice not thicker than 0.3 mm is difficult to get in this way. A thicker slice than necessary to absorb enough light means an insufficiently effective use of material. In other words, lowering costs needs using thinner crystal. In recent years, a method of forming a silicon sheet by spin coating method is proposed, where molten silicon droplets are cast in a mold. However, the resultant sheet is no less than about 0.1 mm to 0.2 mm in thickness. This still is not thinner enough to be crystalline silicon used for absorbing light comparing to 20 to 50μm thickness which is necessary and sufficient for the purpose. Furthermore, a silicon sheet of this thinness is not strong enough to be a substrate any longer. As a result, another substrate is needed as a support for the silicon sheet.
[0004]
[Problem to be solved by the Invention] Considering all these problems, an attempt is proposed, wherein a thin film epitaxial layer is used for a solar cell in order to attain high energy-conversion efficiency and low costs. The thin film epitaxial layer is separated (peeled off) from a single crystalline silicon substrate on which the layer is formed, and is bonded to another substrate (Milnes, A.G. and Feucht, D, L, "Peeled Film Technology Solar Cells", IEEE Photovoltaic Specialist Conference, p. 338, 1975).
[0005] However, according to the above-mentioned method, a SiGe intermediate layer is needed to be inserted between a substrate of single crystalline silicon and an epitaxial-growth layer, to be grown hetero-epitaxially and to be selectively melt to get the growth layer peeled off. In ordinary, in case of forming the layer through the hetero-epitaxial growth, a lattice constant varies, so lattice defects tend to occur at a growth interface. Further, this

method is not necessarily advantageous in terms of process costs, as long as it is necessary to use different sorts of material.

[0006] Another method of forming a thin crystalline film is reported wherein a single crystalline silicon wafer is brought into contact with a surface of an amorphous silicon film deposited on SiO_2, and is processed by heat treatment. Thus, a thin crystalline film is obtained by solid-phase growth (The 38th Meeting of The Japan Society of Applied Physics and Related Societies, Spring 1991, 28p-X-10). According to this method, however, the silicon wafer is bonded so firmly to the solid-phase growth layer that it is difficult to separate them after the growth. This hinders sufficient heat treatment. So, a complete single crystal has not been obtained yet by this method.

[0007]A method according to the present invention aims at overcoming defects of the above-described conventional techniques to obtain high-quality thin film single crystal on a metal substrate. Further, the invention aims at providing a method of manufacturing a satisfactory solar cell using the same.

[0008] An object of the present invention is to provide an inexpensive metal/crystal semiconductor two-layer substrate in such a manner that a non-single crystalline layer formed on a metal substrate is turned into single crystal through solid-phase growth.

[0009] Another object of the present invention is to provide a high-quality solar cell using a single crystal semiconductor.

[0010]

[Means for solving the Problem and Operation] The present invention has been accomplished, as a result of extensive studies made by the inventors of the present application, to solve the problems of the conventional techniques and to attain the above-mentioned objects. The present invention relates to a method of manufacturing a thin single crystal solar cell having satisfactory characteristics, and to a solar cell manufactured thereby. That is, a method of manufacturing a semiconductor substrate having a metal/semiconductor two-layer structure according to the present invention is characterized by including: i) a step of depositing a non-single crystalline silicon layer on a metal substrate; ii) a step of forming a porous surface of a single crystalline silicon substrate; iii) a step of bringing a surface of the non-single crystalline silicon layer on the metal substrate into contact with a surface of a porous layer on the single crystalline silicon substrate; iv) a step of turning the non-single crystalline silicon layer opposing the porous layer into single crystal through solid-phase epitaxial growth by means of heat treatment, and at the same time, forming a silicide layer at an interface between the metal substrate and the non-single crystalline silicon; and v) a step of removing the porous layer through selective etching to separate the single crystalline silicon substrate from a single-crystallized silicon layer on the metal substrate.

[0011] A method of manufacturing a solar cell using a solid-phase epitaxial film according to the present invention is characterized by including: i) a step of depositing a non-single crystalline silicon layer on a metal substrate; ii) a step of forming a porous surface of a single crystalline silicon substrate; iii) a step of bringing a surface of the

non-single crystalline silicon layer on the metal substrate into contact with a surface of a porous layer on the single crystalline silicon substrate; iv) a step of turning the non-single crystalline silicon layer opposing the porous layer into single crystal through solid-phase epitaxial growth by means of heat treatment, and at the same time, forming a silicide layer at an interface between the metal substrate and the non-single crystalline silicon; v) a step of removing the porous layer through selective etching to separate the single crystalline silicon substrate from a single-crystallized silicon layer on the metal substrate; and vi) a step of forming a silicon epitaxial layer on the single-crystallized silicon layer through thin-film epitaxial growth.

[0012] A semiconductor substrate according to the present invention is characterized by being manufactured by executing: i) a step of depositing a non-single crystalline silicon layer on a metal substrate; ii) a step of forming a porous surface of a single crystalline silicon substrate; iii) a step of bringing a surface of the non-single crystalline silicon layer on the metal substrate into contact with a surface of a porous layer on the single crystalline silicon substrate; iv) a step of turning the non-single crystalline silicon layer opposing the porous layer into single crystal through solid-phase epitaxial growth by means of heat treatment, and at the same time, forming a silicide layer at an interface between the metal substrate and the non-single crystalline silicon; and v) a step of removing the porous layer through selective etching to separate the single crystalline silicon substrate from a single-crystallized silicon layer on the metal substrate.

[0013] Further, a solar cell according to the present invention is characterized by being manufactured by executing: i) a step of depositing a non-single crystalline silicon layer on a metal substrate; ii) a step of forming a porous surface of a single crystalline silicon substrate; iii) a step of bringing a surface of the non-single crystalline silicon layer on the metal substrate into contact with a surface of a porous layer on the single crystalline silicon substrate; iv) a step of turning the non-single crystalline silicon layer opposing the porous layer into single crystal through solid-phase epitaxial growth by means of heat treatment, and at the same time, forming a silicide layer at an interface between the metal substrate and the non-single crystalline silicon; v) a step of removing the porous layer through selective etching to separate the single crystalline silicon substrate from a single-crystallized silicon layer on the metal substrate; vi) a step of forming a silicon epitaxial layer on the single-crystallized silicon layer through thin-film epitaxial growth; and vii) a step of forming a semiconductor junction on a surface of the epitaxial layer.

[0014]As shown in Fig. 1, a feature of the present invention is that a surface of a silicon wafer is turned into a porous surface through anodization in an HF solution (Fig. 1a). The surface of amorphous silicon deposited on a metal substrate beforehand and the resultant porous surface are both subjected to heat treatment, and the amorphous silicon is turned into single crystal with the porous portion used as a seed crystal. At the same time, a silicide layer is formed at an interface between the metal substrate and the amorphous silicon to attain a satisfactory ohmic contact (Fig. 1b). The porous layer is removed through selective etching to separate the

silicon wafer from the solid-phase growth layer (Fig. 1c). Further, if needed, an epitaxial layer is deposited into a desired thickness by an ordinary crystal growth method to form a single crystalline silicon thin film on the metal substrate (Fig. 1d).

[0015] The formation of porous silicon through anodization requires holes for anodic reaction. Hence, p type silicon having holes is mainly made porous (T. Unagami, J. Electrochem. Soc., vol. 127, 476 (1980)). However, there is another report that low-resistance n type silicon can be made porous (R. P. Holmstrom and J. Y. Chi, Appl. Phys. Lett., vol. 42, 386 (1983)). Thus, low-resistance silicon can be made porous irrespective of whether the silicon is n type or p type. The porous silicon obtained by anodizing the single crystalline silicon has several hundreds of pores according to a transmission electron microscopic observation. The density thereof is half or less of that of single crystalline silicon. Nevertheless, single crystallinity is maintained. As is well known in the art, an epitaxial layer is formed on the porous silicon through LPCVD for instance. Further, as mentioned above, the porous silicon includes a number of pores as mentioned above, and has a surface area which is drastically increased with respect to its volume. Hence, a chemical etching rate of porous silicon is considerably higher than that of an ordinary single crystalline silicon.

[0016] In addition, NaOH aqueous solution is solely used as selective etchant for ordinary crystalline silicon and for porous silicon in the conventional technique. The selective etching of the porous silicon with the NaOH aqueous solution has a problem in that Na ions are absorbed into the etched surface, which results in contamination with impurities.

[0017] The inventors of the present application have made repeated experiments and found that a non-single crystalline silicon layer, specifically an amorphous silicon layer, which is deposited on a metal substrate, is brought into contact an upper surface of a porous silicon layer, followed by heat treatment, with the result that the non-single crystalline layer is turned into single crystal through solid-phase growth with the porous layer used as seed crystal, and that the porous silicon layer alone can be selectively etched with a mixture of solution of alcohol and hydrogen peroxide solution, and hydrofluoric acid having no function of etching crystalline silicon. As a result, the present invention has been completed based on the findings that a high-quality thin film single crystalline silicon layer can be formed on a metal substrate. Hereinafter, experiments made by the inventors of the present application will be described with reference to Fig. 1.

[0018] (Experiment 1) Formation of porous silicon

A 500 μm-thick p type (100) single crystalline silicon wafer 101 having a specific resistance of 0.01 $\Omega \cdot$cm is subjected to anodization in an HF aqueous solution. Anodization conditions are shown in Table 1.

[0019]

[Table 1]

Applied voltage	2.6 V
Current density	30 mA/cm^2
Anodization solution	HF:H_2O:C_2H_5OH = 1:1:1
Time	1 min

Porous layer thickness	2.5 μm

[0020] As a result of observing a surface of the resultant porous silicon layer 102 with a transmission electron microscope, pores with an average diameter of about 600 Å are formed. Further, as a result of observing a section of the porous silicon layer with a high-resolution scanning electron microscope, minute pores are similarly formed in the vertical direction with respect to the substrate. Further, the density is measured with the anodization time being in the conditions of Table 1 being set longer and with the porous silicon layer thickness being set larger. The measurement result shows that the density of the porous silicon layer is 1.1 g/cm^3, which is about half the density of the single crystalline silicon.

[0021] (Experiment 2) Solid-phase growth with porous silicon used as seed crystal

An amorphous silicon 104 is deposited with the thickness of 0.1 μm on a 0.8 mm-thick W (tungsten) substrate 103 through vacuum evaporation. Then, the surface of the porous silicon layer on the wafer, which is formed in Experiment 1, is brought into contact with an upper surface of the amorphous silicon layer, followed by temporary heat treatment at a temperature lower than the crystallization temperature of the amorphous silicon. Thus, the surface of the porous silicon 102 is put into close contact with the surface of amorphous silicon 104.

[0022] Next, the thus-bonded substrate is subjected to heat treatment at 630°C for a second time to promote the growth of a solid-phase epitaxial layer 106 in the amorphous silicon layer, with the porous silicon 102 being seed crystal. The heat treatment ends after a sufficient amount of time. The observation of the substrate section with the transmission electron microscope reveals that the amorphous silicon layer being in contact with the porous silicon is completely turned into single crystal, while satisfactory crystallinity being maintained.

[0023] Further, as a result of analyzing compositions, it is found that a WSi_2 layer 105 is formed at an interface between the W substrate 103 and the single crystallized silicon layer 106.

[0024] (Experiment 3) Selective etching of porous silicon

An examination is made on etching of the porous silicon manufactured under the same conditions as Experiment 1 with a mixture of hydrofluoric acid, alcohol, and hydrogen peroxide solution.

[0025] Fig. 2 shows a time-varying thickness of porous silicon and single crystalline silicon that are etched by being immersed into a mixture (10:6:50) of 49% hydrofluoric acid, 100% ethyl alcohol, and 30% hydrogen peroxide solution without being stirred. The thickness of the porous silicon and the single crystalline silicon before etching is about 300 μm and 500 μm, respectively.

[0026] The porous silicon and the single crystalline silicon are immersed into the above-described mixture at room temperature to measure how far the thickness is reduced. The measurement result shows that the porous silicon is rapidly etched by 107 μm in about 40 minutes and by up to 244 μm in 80 minutes. The etched surface is extremely even in spite of such a high etching rate. In contrast, the single crystalline

silicon is etched by only 50 Å or less, even in 120 minutes, which reveals that single crystalline silicon is rarely etched.
[0027] Next, the bonded substrate obtained in Experiment 2 is immersed in the mixed etchant described above and is left to stand. Then, only the porous silicon layer 102 is selectively etched to separate the wafer 101 side from the metal substrate 103 side. After being washed with water and dried, the surface of the metal substrate (having opposed the porous layer) is observed with high-resolution scanning electron microscope. Then, a single crystalline silicon layer is formed with the thickness of about 0.1 μm and with an extremely even surface. Further, the wafer surface (having opposed the porous layer) is similarly observed, and is also found to be extremely even.
[0028] As mentioned above, it is revealed that according to the solid-phase growth method using the porous layer as seed crystal, a high-quality single crystalline silicon layer can be formed on the metal substrate.
[0029] Furthermore, the inventors of the present application have made an attempt to manufacture a solar cell using the resultant substrate of a metal/single crystalline silicon two-layer structure.
[0030] (Experiment 4) Crystal growth on solid-phase growth layer

The solid-phase epitaxial layer 106 formed on the metal substrate in Experiment 3 is used to further form an epitaxial layer 107. As a crystal growth method, an ordinary LPCVD method is used, and the growth is promoted under the conditions of Table 2.
[0031] The crystal surface after the crystal growth is observed with optical microscope and with scanning electron microscope. The observation result shows that a flat surface is obtained. The growth layer section is observed with transmission electron microscope. The observation result confirms that a single crystalline epitaxial layer with satisfactory crystallinity is formed.
[0032]
[Table 2]

Gas flow rate	Substrate temperature	Pressure	Growth time
SiH_2Cl_2/H_2 = 0.5/80 ℓ/min	950 °C	80 Torr	160 min

[0033] (Experiment 5) Manufacturing of solar cell

A solar cell is manufactured based on the experimental results of Experiments 1 and 4. Similar to Experiment 1, the porous silicon layer 102 is formed on the silicon wafer 101 under the conditions of Table 1. Next, the 0.1 μm-thick amorphous silicon 104 is deposited on the W substrate 103 through vacuum evaporation using p type porous silicon having ρ= 0.01 Ω·m as an evaporation source. The above-mentioned porous silicon layer 102 is brought into contact with an upper surface of the amorphous silicon layer 104 and into close contact therewith through heat treatment. The bonded substrate is subjected to heat treatment at 630°C to promote solid-phase growth, and thus a solid-phase epitaxial layer is formed. Next, similar to Experiment 3, the substrate is immersed into a mixture of hydrofluoric acid/ethyl alcohol/hydrogen peroxide solution to selectively etch the porous silicon 102 and to

separate the wafer 101 side from the metal substrate 103 side. Under the LPCVD conditions described in Experiment 4, the silicon 107 is formed through epitaxial growth on the solid-phase growth layer 106 A crystalline layer having a thickness of about 50 μm is obtained.

[0034] Subsequently, P ions are implanted from the surface of the formed epitaxial layer at 50 KeV and 1×10^{15} cm^{-2}, and then annealing is successively performed under the conditions of 550°C, 1 hour/800°C, 30 min/550°C, 1 hour for activation of impurities and for recovery from damages of ion implantation. A junction is formed. Finally, a transparent conductive film and a collecting electrode are formed through vacuum evaporation on the epitaxial layer surface. Thus, a solar cell is manufactured.

[0035] A measurement is made of a current-voltage characteristic (I-V characteristic) of the epitaxial thin film solar cell obtained by epitaxial growth on a solid-phase growth layer with the porous portion used as seed crystal, under the illumination with light at AM1.5 (100 mW/cm^2). The measurement result is as follows: an open-circuit voltage is 0.55 V, a short-circuit photocurrent is 31 mA/cm^2, a fill factor is 0.72, and conversion efficiency is 12.3%. In this way, a solar cell having satisfactory crystallinity is obtained.

[0036] As mentioned above, the present invention being completed based on the experimental results described above relates to a method of manufacturing a substrate and to a method of manufacturing a crystalline solar cell. The substrate has a metal/semiconductor two-layer structure obtained by forming a porous layer on a wafer, and turning a non-single crystalline layer on a metal substrate into a single crystalline layer through solid-phase growth with a porous layer used as seed crystal. The solar cell is obtained by forming an additional layer through epitaxial growth on the substrate. A feature of the present invention is that a wafer for forming a porous layer can be reused, and is advantageous in terms of costs.

[0037] In an anodization method for forming a porous silicon layer used in the present invention, a hydrofluoric acid is used. An amount of current that flows during the anodization is appropriately determined based on a HF concentration, a desired thickness of the porous layer. Preferably, the current amount is from several mA/cm^2 to several tens of mA/cm^2. Further, if alcohol such as ethyl alcohol is added to the HF solution, bubbles of a reaction product gas generated during the anodization can be removed immediately from the reaction surface without stirring. Thus, the porous silicon can be formed uniformly and efficiently. The amount of alcohol added is appropriately determined based on the HF concentration and the desired thickness of the porous layer. The additional amount should be carefully determined so as not to excessively reduce the HF concentration.

[0038] As a selective etchant of the porous silicon used in present invention, a mixture of hydrofluoric acid, alcohol, and hydrogen peroxide solution is used. In particular, the addition of the hydrogen peroxide solution accelerates oxidation of silicon, in other words, increases a reaction speed as compared to the case without hydrogen peroxide solution. The ratio of the hydrogen peroxide solution is changed to control the reaction speed. Further, if alcohol

such as ethyl alcohol is added to the HF solution, bubbles of a reaction product gas resulting from the etching can be instantly removed from the etched surface without stirring. Thus, the porous silicon can be etched uniformly and efficiently. Etching conditions such as a concentration ratio between the solutions in the etchant and etching temperature are appropriately determined within such a range that an etching rate of the porous silicon and an etching selection ratio between the porous silicon and ordinary single crystalline silicon fall within a practicable range, and a beneficial effect of the alcohol is not impaired.

[0039] As a metal substrate material used for methods of manufacturing a semiconductor substrate and a solar cell of the present invention, any metal having high conductivity, which is reactable with silicon to form a compound such as silicide is used. Materials such as W, Co, Cr, are representative examples. Needless to say, apart from the above materials, any material added with the metal having the above properties can be used. Accordingly, an inexpensive substrate other than metal can be used. The thickness of the silicide layer is preferably 0.01 to 0.1 μm, though there are no particular limitations.

[0040] As the non-single crystalline silicon layer deposited on the metal substrate in the present invention, amorphous silicon is mainly used, but a polysilicon layer may be used.

[0041] As the temperature for the solid-phase growth of the present invention, which is executed by using the porous silicon of the present invention 500°C or higher is appropriate, and 550°C is more preferable, when amorphous silicon is used as the non-single crystalline layer. However, in the case of using the polysilicon, the temperature of solid-phase growth is 1,000°C or higher, the solid-phase growth being a high-temperature process. This brings about a change in the porous silicon structure, and impairs the above-mentioned characteristics of the enhanced etching. The non-single crystalline silicon is deposited by any of vacuum evaporation, sputtering, LPCVD, plasma CVD, or light CVD.

[0042] As a crystal growth method for forming an epitaxial layer on the solid-phase growth layer in the present invention, there are LPCVD, sputtering, LPCVD, plasma CVD, light CVD, and liquid-phase growth method. Typical examples of material gas used for the vapor phase growth method such as LPCVD, plasma CVD, or light CVD include silanes and halogenated silanes such as SiH_2Cl_2, $SiCl_4$, $SiHCl_3$, SiH_4, Si_2H_6, SiH_2F_2, and Si_2F_6. Further, as carrier gas or as gas for obtaining a reduction atmosphere, which promotes crystal growth, H_2 is added other than the above-mentioned material gas. A mixing ratio between the above-mentioned material gas and hydrogen is appropriately determined as desired in accordance with the forming method, the type of material gas, and the formation conditions. It, however, is preferably within a range of 1 : 10 to 1 : 1000 (introducing flow rate), more preferably 1 : 20 to 1 : 800.

[0043] The temperature and pressure adopted in the crystal growth method used in the present invention vary depending on the formation conditions such as the forming method, the type of the used material gas, and the flow rate of the material gas and H_2. However, the temperature is, for example, preferably set to fall within a range of about 600°C to 1250°C, more preferably is controlled within 650°C to 1200°C as for the ordinary LPCVD. In the case of using the liquid-phase

growth method with Sn as the solvent, the temperature is preferably controlled within a range of 850°C to 1050°C although it varies depending on a solvent type. In addition, in a low-temperature process such as the plasma CVD, the temperature is preferably set to fall within a range of about 200°C to 600°C, more preferably is controlled within a range of 200°C to 500°C.

[0044] Likewise, the pressure is appropriately set within a range of about 10^{-2} Torr to 760 Torr, more preferably within a range of 10^{-1} Torr to 760 Torr.

[0045] Further, the depth of the junction formed with the method of manufacturing a solar cell of the present invention is preferably in a range of 0.05 to 3 μm, more preferably within a range of 0.1 to 1 μm although it varies depending on the amount of impurity being introduced.

[0046]

[Example] Hereinafter, the present invention will be described in more detail by way of concrete embodiments. However, the present invention is not limited to these embodiments at all.

[0047] Example 1

As mentioned above, the semiconductor substrate having a metal/single crystalline silicon two-layer structure is manufactured through the process of Fig. 1 in the same way as in Experiments 1 to 3.

[0048] The 500 μm-thick p type (100) silicon wafer 101 (ρ=0.01 Ω·cm) is subjected to anodization in an HF aqueous solution under conditions of Table 3. Thus, the wafer 101 is made porous to form the porous silicon layer 102.

[0049]

[Table 3]

Applied voltage	2.6 V
Current density	30 mA/cm^2
Anodization solution	HF: H_2O: C_2H_5OH = 1:1:1
Time	2 min
Porous layer thickness	5 μm

[0050] The metal substrate 103 is formed by depositing Mo on an SUS substrate into the thickness of 500 Å through vacuum evaporation. Then, the amorphous silicon layer 104 is deposited into 0.2 μm on the surface thereof using an ordinary LPCVD apparatus. Deposition conditions are shown in Table 4.

[0051]

[Table 4]

Gas flow rate (ccm)	Substrate temperature (°C)	Pressure (Torr)	Growth rate (nm/min)
SiH_4 50	550	0.3	1.8

[0052] Next, the surface of the porous silicon 102 and the surface of the amorphous silicon 104 are superposed and brought into contact, and then heat treatment is carried out at 500°C for 30 minutes to improve adhesion between the wafer and the SUS substrate.

[0053] Subsequently, another heat treatment is carried out at 600°C for 8 hours for promoting the solid-phase epitaxial growth of the amorphous silicon layer 104 with the porous silicon layer 102 used as seed crystal to completely turn the

amorphous silicon layer into single crystal.
[0054] After that, the bonded substrate is immersed into a mixture (10:6:50) of 49% hydrofluoric acid, 100% ethyl alcohol, and 30% hydrogen peroxide solution for selective etching. The porous silicon layer is completely removed to separate the wafer 101 side from the SUS substrate 103 side, then the SUS substrate is washed with water and dried.
[0055] In this way, the 0.1 μm-thick single crystalline silicon layer 106 is formed on the metal substrate 103. The observation of the surface with optical microscope and scanning electron microscope reveals that the single crystalline silicon layer is not affected by the selective etching of the porous silicon.
[0056] Further, the observation of the section with the transmission electron microscope confirms that the silicon layer maintains satisfactory crystallinity, and a $MoSi_2$ layer 105 is formed at an interface between the substrate 103 and the silicon layer 106.
[0057] Example 2

As in Example 1, the semiconductor substrate having a metal/single crystalline silicon two-layer structure is manufactured through the process shown in Fig. 1.
The 500 μm-thick n type (100) silicon wafer 101 (ρ=0.01 Ω·cm) is subjected to anodization in an HF aqueous solution under conditions of Table 2. Thus, the porous silicon layer 102 is formed on the wafer 101.
[0059] Ti is deposited into the thickness of 500 Å through vacuum evaporation on the SUS substrate 103, and then the amorphous silicon layer 104 is deposited into 0.2 μm under conditions of Table 4 on the surface thereof using an ordinary LPCVD apparatus.
[0060] Next, the surface of the porous silicon 102 and the surface of the amorphous silicon 104 are superposed and brought into contact, and then heat treatment is carried out at 500°C for 30 minutes to improve adhesion between the wafer 101 and the SUS substrate 103.
[0061] Subsequently, heat treatment is carried out at 650°C for 6 hours for promoting the solid-phase epitaxial growth of the amorphous silicon layer 104 with the porous silicon layer 102 used as seed crystal to completely turn the amorphous silicon layer into single crystal.
[0062] After that, the bonded substrate is immersed into a mixture (10:6:50) of 49% hydrofluoric acid, 100% ethyl alcohol, and 30% hydrogen peroxide solution for selective etching. The porous silicon layer 102 is completely removed to separate the wafer 101 side from the SUS substrate 103 side, and then the SUS substrate is washed with water and dried.
[0063] In this way, a 0.1 μm-thick single crystalline silicon layer 107 is formed on the metal substrate 103. The observation of the surface with optical microscope and scanning electron microscope reveals that the single crystalline silicon layer is not affected by the selective etching of the porous silicon.
[0064] Further, the observation of the section with the transmission electron microscope confirms that the silicon layer 106 maintains satisfactory crystallinity, and the $TiSi_2$ layer 105 is formed at an interface between the substrate and the silicon layer.
[0065] Example 3

As in Examples 1 and 2, the semiconductor substrate

having a metal/single crystalline silicon two-layer structure is manufactured through the process shown in Fig. 1.

[0066] The 500 μm-thick p type (100) silicon wafer 103 (ρ= 0.01 Ω·cm) is subjected to anodization in an HF aqueous solution under conditions of Table 2. Thus, the porous silicon layer 102 is formed on the wafer.

[0067] Mo is deposited into the thickness of 500 Å through vacuum evaporation on the SUS substrate 103, and then the amorphous silicon layer 104 is deposited into 0.2 μm under conditions of Table 5 on the surface thereof using a plasma CVD apparatus.

[0068]

[Table 5]

Gas flow rate (cc/mm)	Substrate temperature (°C)	Pressure (Torr)	Discharge power (W)
SiH_4 * 10	450	0.3	5

* PH_3 added: $PH_3/SiH_4 = 3\times10^{-4}$

[0069] Next, the porous silicon 102 surface and the amorphous silicon 104 surface are superposed and brought into contact, and then heat treatment is carried out at 500°C for 30 minutes to improve adhesion between the wafer 102 and the SUS substrate 103.

[0070] Subsequently, another heat treatment is carried out at 1200°C for 30 seconds for promoting the solid-phase epitaxial growth of the amorphous silicon layer 104 with the porous silicon layer 102 used as seed crystal through an RTA (Rapid Thermal Annealing) method to completely turn the amorphous silicon layer 104 into single crystal.

[0071] After that, the bonded substrate is immersed into a mixture (10:6:50) of 49% hydrofluoric acid, 100% ethyl alcohol, and 30% hydrogen peroxide solution for selective etching. The porous silicon layer 102 is completely removed to separate the wafer 101 side from the SUS substrate 103 side, and then the SUS substrate 103 is washed with water and dried.

[0072] In this way, the 0.1 μm-thick single crystalline silicon layer is formed on the metal substrate. The observation of the surface with optical microscope and scanning electron microscope reveals that the single crystalline silicon layer is not affected by the selective etching of the porous silicon.

[0073] Further, the observation of the section with the transmission electron microscope confirms that the silicon layer maintains satisfactory crystallinity, and the $MoSi_2$ layer 105 is formed at an interface between the substrate and the silicon layer.

[0074] Example 4

As in Examples 1 and 2, the semiconductor substrate having a metal/single crystalline silicon two-layer structure is manufactured through the process shown in Fig. 1, and crystal is formed through epitaxial growth thereon to manufacture a solar cell.

[0075] The 500 μm-thick n type (100) silicon wafer 101 (ρ=0.01 Ω·cm) is subjected to anodization in a HF aqueous solution under conditions of Table 2. Thus, the porous silicon layer 102 is formed by making the wafer 101 porous.

[0076] Ti is deposited into the thickness of 500 Å through vacuum evaporation on the SUS substrate 103, and then the

amorphous silicon layer 104 is deposited into 0.2 μm on the surface thereof through vacuum evaporation using an n type polysilicon with ρ = 0.001 Ω·cm as an evaporation source.
[0077] Next, the surface of the porous silicon 102 and the surface of the amorphous silicon 104 are superposed and brought into contact, and then heat treatment is carried out at 500°C for 30 minutes to improve adhesion between the wafer 102 and the SUS substrate 103.
[0078] Subsequently, another heat treatment is carried out at 650°C for 6 hours for promoting the solid-phase epitaxial growth of the amorphous silicon layer 104 with the porous silicon layer 102 used as seed crystal to completely turn the amorphous silicon layer 104 into single crystal.
[0079] After that, the bonded substrate is immersed into a mixture (10:6:50) of 49% hydrofluoric acid, 100% ethyl alcohol, and 30% hydrogen peroxide solution for selective etching. The porous silicon layer 102 is completely removed to separate the wafer 101 side from the SUS substrate 103 side, and then the SUS substrate is washed with water and dried.
[0080] A LPCVD apparatus is used for epitaxial growth under the formation conditions shown in Table 6 to thereby form the silicon 107 with the film thickness of about 50 μm.
[0081]
[Table 6]

Gas flow rate (ℓ/min)	Substrate temperature (°C)	Pressure (Torr)	Growth time (min)
SiH_2Cl_2/H_2 * =0.5/80	950	80	160

* PH_3 added: $PH_3/SiH_2Cl_2 = 3\times10^{-6}$

[0082] Next, B is thermally diffused at the temperature of 950°C with BCl_3 used as a diffusion source to form a p+ layer on the surface of the epitaxial layer 107 to obtain a junction depth of about 0.5 μm. A dead layer on the surface of the formed p+ layer is subjected to wet oxidization, and then the junction depth of about 0.2 μm with an appropriate surface concentration is obtained through etching.
[0075] Finally, an ITO transparent conductive film (820 Å)/collecting electrode (Cr/Ag/Cr (200 Å /1 μm/400 Å)) are formed on the p+ layer through EB (Electron Beam) evaporation.
[0076] A measurement is made of the I-V characteristic of the thin-filmed crystalline solar cell thus obtained under the illumination with light at AM1.5 (100 mW/cm^2). The measurement result is as follows: an open-circuit voltage is 0.59 V, a short-circuit photocurrent is 31 mA/cm^2, a fill factor is 0.74, and conversion efficiency is 13.5%. In this way, the solid-phase growth is promoted with the porous silicon as seed crystal, and the epitaxial layer is further formed on the solid-phase growth layer, whereby the thin-film crystalline solar cell having satisfactory crystallinity can be manufactured.
[0085] Example 5
The thin crystalline solar cell is manufactured as described in Example 4.
[0086] The 500 μm-thick p type (100) silicon wafer 101 (ρ = 0.01 Ω·cm) is subjected to anodization in a HF aqueous solution under conditions of Table 2. Thus, the porous silicon layer 102 is formed on the wafer.
[0087] Mo is deposited into the thickness of 500 Å through

vacuum evaporation on the SUS substrate 103, and then the amorphous silicon layer 104 is deposited into 0.2 μm thickness on the surface thereof through vacuum evaporation using an n-type polysilicon with ρ = 0.001 Ω·cm as an evaporation source.
[0088] Next, the surface of the porous silicon 102 and the surface of amorphous silicon 104 are superposed and are brought into contact, and then heat treatment at 500°C for 30 minutes to improve adhesion between the wafer 102 and the SUS substrate 103.
[0089] Subsequently, another heat treatment is carried out at 600°C for 8 hours for promoting the solid-phase epitaxial growth of the amorphous silicon layer 104 with the porous silicon layer 102 used as seed crystal to completely turn the amorphous silicon layer 104 into single crystal.
[0090] After that, the bonded substrate is immersed into a mixture (10:6:50) of 49% hydrofluoric acid, 100% ethyl alcohol, and 30% hydrogen peroxide solution for selective etching. The porous silicon layer 102 is completely removed to separate the wafer 101 side from the SUS substrate 103 side, and then the SUS substrate is washed with water and dried.
[0091] A LPCVD apparatus is used for epitaxial growth under the formation conditions shown in Table 7 to thereby form the silicon layer 107 with the film thickness of about 50 μm.
[0092]
[Table 7]

Gas flow rate (ℓ/min)	Substrate temperature (°C)	Pressure (Torr)	Growth time (min)
SiH_2Cl_2/H_2 * =0.5/80	950	80	160

* B_2H_6 added: $B_2H_6/SiH_2Cl_2 = 2\times10^{-6}$
PSG is deposited into 6000 Å using an atmospheric pressure CVD, and P is thermally diffused at the temperature of 950°C with PSG used as a diffusion source to form an n+ layer with the thickness of 0.1 μm. Subsequently, PSG is removed through etching, and then an ITO transparent conductive film (820 Å)/collecting electrode (Cr/Ag/Cr (200 Å /1 μm/400 Å)) are formed on the n+ layer.
[0093] A measurement is made of the I-V characteristic of the thin film crystalline solar cell thus obtained under the illumination with light at AM1.5 (100 mW/cm^2). The measurement result is as follows: an open-circuit voltage is 0.58 V, a short-circuit photocurrent is 30 mA/cm^2, a fill factor is 0.77, and conversion efficiency is 13.4%.
[0094] Example 6
The p+μe-Si/crystalline silicon hetero solar cell is manufactured as in the case with Examples 4 and 5.
[0095] The substrate manufactured in Example 3 is used to form a silicon layer with the thickness of about 50 μm through the epitaxial growth under the formation conditions of Table 6 using the LPCVD apparatus.
[0096] On the epitaxial layer, p type μe-Si is deposited into the thickness of 200 Å using an ordinary plasma CVD apparatus under conditions of Table 8. At this time, a dark conductivity of the μe-Si is 10S·cm^{-1}.
[0097]
[Table 8]

Gas flow rate	Substrate temperature	Pressure	Discharge power

SiH_4/H_2 = 1 cc/20 cc B_2H_6/SiH_4 = 2.0×10^{-3}	250°C	0.5 Torr	20 W

[0098] In this way, the hetero pn junction is formed, and then ITO is deposited into about 850 Å as a transparent conductive film thereon through electron beam evaporation. Further, a collecting electrode (200 Å/1 μm/400 Å) is formed thereon.
[0099] A measurement is made of the I-V characteristic of the p+ μe-Si/crystalline silicon hetero solar cell thus obtained under the illumination with light at AM1.5. The measurement result is as follows: an open-circuit voltage is 0.62 V, a short-circuit photocurrent is 32 mA/cm^2, a fill factor is 0.7, and conversion efficiency is as high as 13.9%. As mentioned above, according to the present invention, a high-quality silicon layer can be formed on a metal substrate, whereby a high-quality and inexpensive solar cell can be manufactured.
[0100] As has been described above, according to the present invention, the thin film crystalline solar cell having a satisfactory characteristic can be formed on a metal substrate. Hence, mass-productive inexpensive and high-quality thin solar cells can be supplied into the market.

[Brief Description of the Drawings]

[Fig. 1] A schematic diagram illustrating a manufacturing process for a semiconductor substrate according to the present invention.

[Fig. 2] A graph showing a time-varying thickness of porous silicon and single crystalline silicon etched with a selective etchant.

[Description of Reference Numerals]

101 silicon wafer
102 porous silicon layer
103 metal substrate
104 non-single crystalline silicon layer
105 silicide layer
106 solid-phase epitaxial layer
107 epitaxial silicon layer

Fig.1

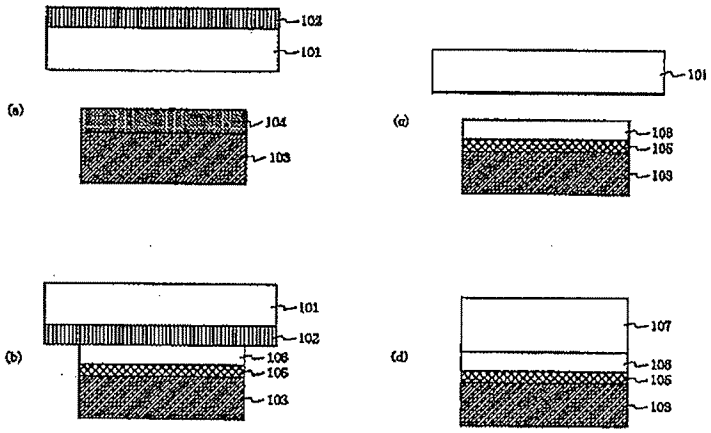
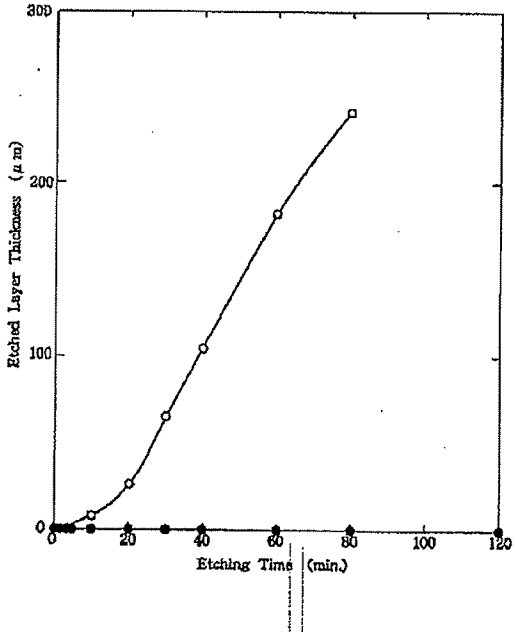

(a)
102
101
104
103
(b)
101
102
106
105
103
(c)
101
108
105
103
(d)
107
108
105
109

Fig.2


300
200
100
0
Etched Layer Thickness (μm)
0
20
40
60
80
100
120
Etching Time (min.)